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Enclosed herewith for filing is the following utility patent application:

Applicant: Uri Cohen

Title of Application: Seed Layers for Interconnects and Methods for Fabricating Such Seed Layers

Pages of specification: 21 Sheets of drawing: 2.

PATENT APPLICATION FILING FEE CALCULATION

	No. Filed	Less	Rate/Claim	Fee
Total Claims	38	- 20	$9.00	$162.00
Independent Claims	5	- 03	$39.00	$ 78.00
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		TOTAL FILING FEE		$620.00

My check in the amount of the total filing fee is enclosed herewith.

Also enclosed herewith for filing in connection with the enclosed application are:

a Declaration, an Information Disclosure Statement, and a Verified Statement Claiming Small Entity Status.

Respectfully submitted,

Dated: October 2, 1999

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UC:pc
Enc.

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Date: 10/2/99

Uri Cohen

VERIFIED STATEMENT CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) and 1.27(b)) -- INDEPENDENT INVENTOR	Docket Number (optional) Seed

Applicant or Patentee: Uri Cohen

Serial or Patent No.: _____

Filed or Issued: _____

Title: Seed Layers for Interconnects and Methods for Fabricating Such Seed Layers

As a below named inventor, I hereby declare that I qualify as an independent inventor as defined in 37 CFR 1.9(c) for purposes of paying reduced fees under Sections 41(a) and (b) of Title 35, United States Code, to the Patent and Trademark Office with regard to the invention described in:

- x the specification filed herewith with title as listed above
- ___ the application identified above
- ___ the patent identified above

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Each person, concern or organization to which I have assigned, granted, conveyed or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention is listed below:

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Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

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Application Information

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Continuity Information

This application is a ::
> Application One ::
Filing Date ::
Patent Number ::

which is a ::
>> Application Two ::
Filing Date ::
Patent Number ::

Seed Layers for Interconnects and Methods for Fabricating Such Seed Layers

Technical Field of the Invention

The present invention pertains to the field of electroplating metals or alloys for filling high aspect ratio openings, such as trenches and vias, for semiconductor metallization interconnects, thin film heads, or micromachined Microelectromechanical Systems (MEMS) devices. In particular, embodiments of the present invention provide improved seed layers for electroplating copper or silver interconnects in semiconductor devices and methods for fabricating such improved seed layers. The improved seed layers facilitate reliable, void-free filling of small openings with high aspect ratios for so called "Damascene" and "Dual Damascene" copper and/or silver interconnects.

Background of the Invention

As is well known in the prior art, filling trenches and/or vias formed on a wafer by electroplating copper metal to form semiconductor device interconnects (often referred to as a "Damascene" or a "Dual Damascene" process), requires that a metallization layer (often referred to in the art as a seed layer or a base layer) be formed over the wafer surface. As is also well known in the prior art, the seed layer is required: (a) to provide a low-resistance electrical path (to enables uniform electroplating over the wafer surface); (b) to adhere well to the wafer surface (usually to an oxide-containing a dielectric film such as SiO_2, SiO_X, or SiO_XN_Y); and (c) to be compatible with subsequent electroplating copper thereon.

As is well known, the requirement of providing a low-resistance electrical path is fulfilled by choosing the seed layer to be comprised of an adequately thick, low-resistivity material.

As is further well known, since copper has a rather poor adhesion to oxide surfaces, the requirement of adhering well to the wafer surface is typically fulfilled by

disposing an intermediary barrier (or adhesion) metallic layer having a strong affinity for oxygen atoms under the seed layer. As is well known in the prior art, the barrier metallic layer is formed prior to the seed layer to provide good adhesion: (a) to the oxide surface underneath it (the barrier layer provides good adhesion to the oxide surface by sharing oxygen atoms) and (b) to the seed layer above it (the barrier metallic layer provides good adhesion to the seed layer by metal to metal bonds). The barrier layer is often also referred to as an "adhesion layer" or a "liner". In addition to providing good adhesion, the barrier layer also serves to mitigate copper out-diffusion directly into the device, or indirectly (through an insulating or a dielectric layer) into the device. As is well known in the prior art, the barrier layer is usually chosen from the refractory metals or their alloys, such as for example, Ta, TaN_X, Cr, CrN_X, Ti, TiN_X, W, WN_X, and other alloys containing one or more of these materials.

As is still further well known, the requirement of being compatible with electroplating copper is fulfilled by choosing a seed layer that does not react spontaneously (i.e., by displacement) with copper electrolyte used during the electroplating. This is satisfied by requiring that the seed layer does not comprise a metal or alloy that is less noble than copper.

Typically, a seed layer comprises a copper layer that is deposited by a "dry" technique, such as by physical vapor deposition ("PVD"), including but not limited to sputtering or evaporation, or by chemical vapor deposition ("CVD"). However, the seed layer may also be deposited by a "wet" electroless plating process. In such cases, the copper seed layer thickness is typically in a range of about 300Å to about 2,000Å on the field (i.e., the top surface of the wafer outside trenches and via openings). In such cases, the barrier layer is typically deposited to a thickness of about 50Å to about 500Å (on the field) by either a PVD or a CVD technique.

The PVD techniques include, for example and without limitation, techniques such as evaporation and various sputtering techniques, such as DC and/or RF plasma sputtering, bias sputtering, magnetron sputtering, ion plating, or Ionized Metal Plasma (IMP) sputtering. As is well known in the art, in general, due to their anisotropic

and directional ("line of sight") nature, the PVD techniques produce non-conformal deposition. The CVD techniques include, for example and without limitation, thermal CVD, Plasma Enhanced CVD ("PECVD"), Low Pressure CVD ("LPCVD"), High Pressure CVD ("HPCVD"), and Metal Organo CVD ("MOCVD"). For example, one precursor used for CVD Cu is Cupraselect™ which is a precursor of Schumacher, Inc. As is well known in the art, in general, due to their isotropic and non-directional nature, the CVD and the electroless techniques produce conformal deposition, with substantially uniform thickness over the entire surface, including over the field and the bottom and sidewall surfaces of the openings.

Aspect ratio ("AR") is typically defined as a ratio between a vertical dimension, D (depth), of an opening and its smallest lateral dimension, W (width, or diameter): AR = D/W. Usually, in electroplating metals or alloys to fill patterns having high aspect ratio openings (for example, in an insulator or a dielectric), the electroplating rate inside openings is slower than the rate outside openings (i.e., on the field). Further, the higher the AR of the openings, the slower the electroplating rate is inside. This results in poor or incomplete filling (voids) of high AR openings, when compared with results achieved with low AR openings. To overcome this problem in the prior art, commercial copper electrolytes contain additives that adsorb and locally inhibit (or suppress) growth outside the openings (i.e., on the field). Further, growth inhibition inside the openings is decreased from that achieved outside the openings due to slow replenishment of the additives inside the openings as compared with replenishment of the additives on the field. As a result, the deposition rate inside the openings is faster than outside, thereby facilitating void-free copper fill. Other well known reasons for voids in copper electrofill include discontinuous (or incomplete coverage of) seed layers inside the openings, and pinching-off of opening walls (for example, by overhangs of the top corners) prior to plating.

The openings may consist of vias, trenches, or patterned photoresist. As is well known, in damascene or dual damascene processes, an insulating or a dielectric layer is pattern-etched to form openings therein. Next, a barrier (or an adhesion) metallic layer

and a seed layer are deposited over the insulating layer to metallize its field (the surface surrounding openings), as well as the sidewalls and bottom surfaces of the openings. Next, copper electroplating is performed over the entire metallized surface, including the top surface (the field) surrounding the openings, and inside the patterned openings. Finally, excess plated copper overlying the openings and the top surface (the field) of the insulating layer, as well as the barrier and seed layers on the field, are removed, for example, by a mechanical polishing or by a chemical mechanical polishing ("CMP") technique. The end result is copper filled openings (trenches and vias), including bottom and sidewall surfaces lined by the barrier and seed layers. In today's most advanced copper filling processes for trenches and vias, the openings have ARs as high as 5:1 (D = 1.25μm; W = 0.25μm). Future trenches and vias openings will likely require W = 0.13 - 0.18μm, or narrower, and AR = 6:1 - 10:1, or larger.

As semiconductor device dimensions continue to shrink, there is an ever increasing demand for narrower interconnect cross-sections and, thus, smaller openings and larger aspect ratios (AR) during the copper electrofill. To ensure void-free copper filling, the seed layer inside the openings must completely cover the bottom and the sidewall surfaces inside the openings without discontinuities, or else there will be voids in the copper electrofill. On the other hand, the seed layer must not be so thick on the sidewalls that it pinches-off the very narrow openings and should not overhang the top corners of the openings so that it pinches-off the very small openings. Similarly, the barrier layer must also be continuous inside the openings. In contrast to these requirements with respect to the openings, the seed layer must be sufficiently thick on the top surface (the field) to provide a low-resistive electrical path that facilitates uniform plating across the surface of the wafer. That is, the seed layer must be sufficiently thick on the field to avoid radial non-uniformity across the wafer caused by a voltage (or IR) drop between a contact at the edge of the wafer to the center of the wafer. Any voltage drop (and resulting non-uniformity therefrom) becomes more severe as the resistance of the seed layer increases due to high resistivity and/or insufficient thickness. To ensure a sufficiently low-resistance seed layer, it is now common to deposit a copper seed layer to a thickness of

about 1,000Å to about 2,000Å on the top surface (field) by a PVD technique, or to a thickness of about 300Å to about 1,000Å by a CVD technique.

However, neither of these techniques satisfies all of the above-identified requirements. The non-conformal PVD techniques, while providing adequate thickness on the field, fail to provide continuous and complete step coverage inside very narrow openings with large AR. They also result in substantial overhangs at the top corners of the openings. The conformal CVD or electroless techniques, on the other hand, while providing continuous and complete step coverage of the seed layer inside very narrow openings, pinch-off the small openings when used at thicknesses required on the field for a low-resistance electrical path. As a result, typical conformal CVD or electroless seed layers are too thin on the field and too thick inside the very narrow openings.

As one can readily appreciate from the above, a need exists in the art for a method for void-free copper filling of very narrow openings having high aspect ratios.

Summary of the Invention

Embodiments of the present invention advantageously satisfy the above-identified need in the art and provide a method for void-free copper or silver filling of small openings having high aspect ratios.

One embodiment of the present invention is a method for making metallic interconnects comprising: (a) forming a patterned insulating layer on a substrate, the patterned insulating layer including at least one opening and a field surrounding the at least one opening; (b) depositing a barrier layer over the field and inside surfaces of the at least one opening; (c) depositing a first seed layer over the barrier layer using a first deposition technique; (d) depositing a second seed layer over the first seed layer using a second deposition technique, the first and second deposition techniques being different; and (e) electroplating a metallic layer over the second seed layer, the electroplated metallic layer comprising a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals.

Brief Description of the Figures

FIG. 1 shows a cross-sectional view of an inventive structure formed in accordance with a preferred embodiment of the present invention wherein a first, conformal seed layer is deposited over a barrier layer, followed by a second, non-conformal seed layer deposited over the first, conformal seed layer;

FIG. 2 shows a cross-sectional view of the inventive structure of FIG. 1 after removing excess plated copper or silver overlying an opening and the field, as well as removing the seed layers and barrier layer overlying the field surrounding the opening;

FIG. 3 shows a cross-sectional view of an inventive structure formed in accordance with an alternative embodiment of the present invention wherein a first, non-conformal seed layer is deposited over a barrier layer, followed by a second, conformal seed layer deposited over the first, non-conformal seed layer; and

FIG. 4 shows a cross-sectional view of the inventive structure of FIG. 3 after removing excess plated copper or silver overlying an opening and the field, as well as removing the seed layers and barrier layer overlying the field surrounding the opening.

Detailed Description

FIG. 1 shows a cross-sectional view of an inventive structure formed in accordance with a preferred embodiment of the present invention wherein a first, conformal seed layer is deposited over a barrier layer, followed by a second, non-conformal seed layer deposited over the first, conformal seed layer. The conformal seed layer provides continuous and complete step coverage inside the openings, while the non-conformal seed layer provides a low resistance electrical path over the top surface (field) surrounding the openings to enable uniform plating across the substrate (or wafer).

In accordance with the preferred embodiment of the inventive method of the present invention, barrier layer 18 is deposited over the entire surface of wafer 10, including over patterned insulating layer 12 (having had opening 16 patterned therein in

accordance with any one of a number of methods that are well known to those of ordinary skill in the art), using a conformal Chemical Vapor Deposition ("CVD") technique. Although the term barrier layer is used, it should be understood by those of ordinary skill in the art that the term barrier layer includes examples wherein: (a) the barrier layer acts both as an adhesion layer and as a barrier layer; (b) a barrier layer separate from an adhesion layer is used; and (c) a multiplicity of layers is used, some acting as adhesion layers, some acting as barrier layers, or some acting as both. Further, although the term wafer is used, this also includes the term substrate as it is used in the art. Still further, although the present invention is described in the context of opening 16, in practice, a multiplicity of openings are patterned and filled in accordance with the present invention.

Advantageously, in accordance with the present invention, the use of a CVD technique to deposit barrier layer 18 ensures substantially complete and continuous coverage of the bottom and sidewall surfaces inside opening 16. However, it is within the scope of the present invention that barrier layer 18 may also be deposited using a Physical Vapor Deposition ("PVD") technique that provides continuous bottom and sidewall coverage. In accordance with the present invention, barrier layer 18 may comprise, for example and without limitation, a material selected from Ta, TaN_X, Cr, CrN_X, Ti, TiN_X, W, WN_X, and other alloys containing one or more of these materials. Further, the thickness of barrier layer 18 can be in a range of about 30Å to about 500Å, and more preferably in a range of about 50Å to about 300Å. Since barrier layer 18 occupies a certain fraction of interconnects formed in accordance with the present invention, and since barrier layer 18 has a relatively large resistivity, its thickness should be minimized. However, the thickness of barrier layer 18 should be sufficiently large to mitigate copper out-diffusion and to provide complete bottom and sidewall coverage inside opening 16. Many CVD techniques and PVD techniques are well known to those of ordinary skill in the art for forming barrier layer 18.

Next, conformal seed layer 20 is deposited over barrier layer 18. Conformal seed layer 20 can be preferably deposited by using a CVD technique, but it can also be deposited by using an electroless technique. Many CVD techniques and electroless

techniques are well known to those of ordinary skill in the art for forming conformal seed layer 20. The thickness of conformal seed layer 20 can be in a range of about 50Å to about 500Å, and more preferably in a range of about 100Å to about 300Å. Finally, non-conformal seed layer 22 is deposited over conformal seed layer 20. Non-conformal seed layer 22 can be preferably obtained using a PVD technique. Many PVD techniques are well known to those of ordinary skill in the art for forming non-conformal seed layer 22. The thickness of non-conformal seed layer 22 can be in a range of about 100Å to about 2,000Å, and more preferably in a range of about 300 Å to about 1,000Å (in the field).

In accordance with the present invention, the conformal and non-conformal seed layers may comprise the same material, or they may comprise different materials. Although copper is commonly used as a seed layer, a highly conductive silver (Ag) layer can also be used. In fact, Ag has lower resistivity than that of Cu and, therefore, can be formed with a smaller thickness than that required when using Cu. Thus, conformal seed layer 20 and non-conformal seed layer 22 may comprise, for example, a material selected from Cu, Ag, or alloys comprising one or more of these metals.

Due to the non-directional, isotropic nature of CVD deposition techniques, the thickness of the CVD layers is substantially uniform over the entire surface (i.e., conformal), including over field 14, and over bottom and sidewall surfaces inside opening 16. In reality, however, even the best conformal CVD layers are thicker over the field than inside the openings. In fact, it is quite common for CVD Cu seed layers inside openings to have a thickness of about 80% of that over the field. In addition, the thickness of a CVD barrier layer inside the openings is typically only about 50% of that over the field. Thus, even the best CVD layers exhibit some overhang at the top corners of the openings.

The following presents an example of a preferred embodiment of the inventive method for 0.18μm wide vias or trenches. In accordance with the preferred embodiment, one deposits, by a CVD technique, a barrier layer comprised of about 200Å of TaN or WN, then one deposits, by a CVD technique, a conformal seed layer comprised of about 300Å of Cu, finally one deposits, by a PVD technique, a non-conformal seed layer comprised of about 600Å of Cu (as measured on the field). This will result in a total

combined thickness of about 400Å inside the openings: {Cu(PVD~50Å)/Cu(CVD~250Å)/TaN(CVD~100Å)} and a combined Cu seed layer thickness of about 900Å on the field: {Cu(PVD~600Å)/Cu(CVD~300Å)/TaN(CVD~200Å}. Advantageously, in accordance with the present invention, the inventive "two-step" seed layer deposition ensures a continuous seed layer having excellent step coverage, and a low-resistance electrical path on the field to ensure uniform copper plating across the wafer. It may be noted that although the combined thickness of the copper seed layers inside the openings is only about 300Å, due to the very short distance to the field (typically about 1μm), a voltage drop from the field to the inside of the openings is negligible. Thus, the thickness of the "two-step" seed layer inside the openings is adequate for copper plating therein. In fact, if necessary, the thickness of the "two-step" seed layer inside the openings can be further decreased (to a range from about 100Å to about 200Å) to enable void-free copper filling of even smaller openings (for example, 0.13μm). In the above example, the combined thicknesses of the barrier and seed layers at the sidewalls of the openings is about 400Å on each side, thus occupying about 800Å of the 1,800Å opening. This leaves enough room (~1,000Å) to facilitate electroplating inside the opening without sealing or pinching-off of the top corners.

After depositing seed layers 20 and 22 shown in FIG. 1, substrate 10 is placed in a copper electroplating bath, and electroplating is carried out in accordance with any one of a number of methods that are well known to those of ordinary skill in the art to deposit a thickness of copper sufficient to fill patterned opening 16, with some excess, and to cover field 14 surrounding opening 16. Finally, excess plated copper overlying opening 16 and overlying field 14, as well as seed layers 20 and 22 and barrier layer 18 overlying field 14, are removed using any one of a number of techniques that are well known to those of ordinary skill in the art, for example, using a mechanical polishing or a chemical mechanical polishing (CMP) technique. Other removal techniques, such as wet or dry etching techniques may also be used to remove excess plated copper overlying opening 16 and field 14, and to remove seed layers 20 and 22 and barrier metallic layer 18 overlying

field 14. It should be clear to those of ordinary skill in the art that removal may also be accomplished using a combination of techniques, including those identified above.

Although the detailed description above refers to filling opening 16 by electroplating copper, it is within the scope of the present invention to electrofill opening 16 with any low resistivity material, such as a material selected from Cu, Ag, or an alloy comprising one or more of these metals. In fact, silver (Ag) has lower resistivity than that of Cu, and may be attractive for further reducing the dimensions of the interconnects.

FIG. 2 shows a cross-sectional view of the inventive structure of FIG. 1 after removing excess plated copper (or silver) 24 overlying opening 16 and field 14, and removing seed layers 20 and 22 and barrier layer 18 overlying field 14 surrounding opening 16. FIG. 2 illustrates the filling of openings (trenches and vias) with electroplated copper (or silver) 24, as well as the lining of the bottom and sidewall surfaces of opening 16 by barrier layer 18 and seed layers 20 and 22. As shown in FIG. 2, all metallic layers were removed from field 14 of insulating layer 12 which surrounds embedded electroplated copper (or silver) interconnect 24.

FIG. 3 shows a cross-sectional view of an inventive structure formed in accordance with an alternative embodiment of the present invention wherein a first, non-conformal seed layer is deposited over a barrier layer, followed by a second, conformal seed layer deposited over the first, non-conformal seed layer. The non-conformal seed layer provides a low resistance electrical path over the top surface (field) surrounding the openings to enable uniform plating across the substrate (or wafer), while the conformal seed layer provides continuous and complete step coverage inside the openings.

In accordance with the alternative embodiment of the inventive method of the present invention, barrier layer 118 is deposited over the entire surface of wafer 110, including over patterned insulating layer 112 (having had opening 116 patterned therein in accordance with any one of a number of methods that are well known to those of ordinary skill in the art), using a conformal Chemical Vapor Deposition ("CVD") technique. Although the term barrier layer is used herein, it should be understood by those of ordinary skill in the art that the term barrier layer includes examples wherein: (a) the barrier layer

acts both as an adhesion layer and as a barrier layer; (b) a barrier layer separate from an adhesion layer is used; and (c) a multiplicity of layers is used, some acting as adhesion layers, some acting as barrier layers, or some acting as both. Further, although the term wafer is used, this also includes the term substrate as it is used in the art. Still further, although the present invention is described in the context of opening 116, in practice, a multiplicity of openings are patterned and filled in accordance with the present invention.

Advantageously, in accordance with the present invention, the use of a CVD technique to deposit barrier layer 118 ensures complete and continuous coverage of the bottom and sidewall surfaces inside opening 116. However, it is within the scope of the present invention that barrier layer 118 may also be deposited using a Physical Vapor Deposition ("PVD") technique that provides continuous bottom and sidewall coverage. In accordance with the present invention, barrier layer 118 may comprise, for example and without limitation, a material selected from Ta, TaN_X, Cr, CrN_X, Ti, TiN_X, W, WN_X, and other alloys containing one or more of these materials. Further, the thickness of barrier layer 118 can be in a range of about 30Å to about 500Å, and more preferably in a range of about 50Å to about 300Å. Since barrier layer 118 occupies a certain fraction of interconnects formed in accordance with the present invention, and since barrier layer 118 has a relatively large resistivity, its thickness should be minimized. However, the thickness of barrier layer 118 should be sufficiently large to mitigate copper out-diffusion and to provide complete bottom and sidewall coverage inside opening 116. Many CVD techniques and PVD techniques are well known to those of ordinary skill in the art for forming barrier layer 118.

Next, non-conformal seed layer 126 is deposited over barrier layer 118. Non-conformal seed layer 126 can be preferably obtained using a PVD technique. Many PVD techniques are well known to those of ordinary skill in the art for forming non-conformal seed layer 126. The thickness of non-conformal seed layer 126 can be in a range of about 100Å to about 2,000Å, and more preferably in a range of about 300Å to about 1,000Å (on the field). Finally, conformal seed layer 128 is deposited over non-conformal seed layer 126. Conformal seed layer 128 can be preferably obtained using a CVD or

electroless technique. Many CVD techniques and electroless techniques are well known to those of ordinary skill in the art for forming conformal seed layer 128. The thickness of conformal seed layer 128 can be in a range of about 50Å to about 500Å, and more preferably in a range of about 100Å to about 300Å.

In accordance with the present invention, the conformal and non-conformal seed layers may comprise the same material, or they may comprise different materials. Although copper is commonly used as a seed layer, a highly conductive silver (Ag) layer can also be used. Non-conformal seed layer 126 and conformal seed layer 128 may comprise, for example, a material selected from Cu, Ag, or alloys comprising one or more of these metals.

After depositing seed layers 126 and 128 shown in FIG. 3, substrate 110 is placed in a copper electroplating bath, and electroplating is carried out in accordance with any one of a number of methods that are well known to those of ordinary skill in the art to deposit a thickness of copper sufficient to fill patterned opening 116, with some excess, and to cover field 114 surrounding opening 116. Finally, excess plated copper overlying opening 116 and field 114 of insulating layer 112, as well as seed layers 126 and 128 and barrier layer 118 overlying field 114, are removed using any one of a number of techniques that are well known to those of ordinary skill in the art, for example, using a mechanical polishing or a chemical mechanical polishing (CMP) technique. Other removal techniques, such as wet or dry etching techniques may also be used to remove excess plated copper overlying opening 116 and field 114, and to remove seed layers 126 and 128 and barrier layer 118 overlying field 114. It should be clear to those of ordinary skill in the art that removal may also be accomplished using a combination of techniques, including those identified above.

Although the detailed description above refers to filling opening 116 by electroplating copper, it is within the scope of this invention to electrofill opening 116 with any low resistivity material, such as a material selected from Cu, Ag, or alloys comprising one or more of these metals. In fact, silver (Ag) has lower resistivity than that of Cu, and may be attractive for further reducing the dimensions of the interconnects.

FIG. 4 shows a cross-sectional view of the inventive structure of FIG. 3 after removing excess electroplated copper (or silver) 130 overlying opening 116 and field 114, and removing seed layers 126 and 128 and barrier layer 118 overlying field 114 surrounding opening 116. FIG. 4 illustrates the filling of openings (trenches and vias) with electroplated copper (or silver) 130, as well as the lining of the bottom and sidewall surfaces of opening 116 by barrier layer 118 and seed layers 126 and 128. As shown in FIG. 4, all metallic layers were removed from field 114 of insulating layer 112 which surrounds embedded electroplated copper (or silver) interconnect 130.

It should be understood that the scope of the present invention is not limited to the embodiments described above with respect to FIG. 1 and FIG. 3. For example, in accordance with further embodiments of the present invention, a thin ("Flash") PVD seed layer can be deposited first, followed by a conformal CVD or electroless seed layer, and finally followed by a (relatively thick) PVD seed layer to produce three separately deposited seed layers. Another three-step combination may include a first deposited CVD seed layer, followed by a relatively thick PVD seed layer, and finally followed by a second deposited CVD seed layer. Other combinations may comprise even more steps in the deposition of the seed layer. In accordance with one aspect of the present invention, the first PVD Flash seed layer may serve to enhance adhesion to the barrier layer and/or to improve grain morphology of a subsequently deposited CVD seed layer. In this embodiment, the three (or more) separately deposited seed layers may comprise the same metal or alloy or they may comprise, for example and without limitation, different materials chosen from Cu, Ag, or alloys comprising one or more of these metals.

Those skilled in the art will recognize that the foregoing description has been presented for the sake of illustration and description only. As such, it is not intended to be exhaustive or to limit the invention to the precise form disclosed.

What is claimed is:

1. A method for making metallic interconnects comprising:

forming a patterned insulating layer on a substrate, the patterned insulating layer including at least one opening and a field surrounding the at least one opening;

depositing a barrier layer over the field and inside surfaces of the at least one opening;

depositing a first seed layer over the barrier layer using a first deposition technique;

depositing a second seed layer over the first seed layer using a second deposition technique, the first and second deposition techniques being different; and

electroplating a metallic layer over the second seed layer, the electroplated metallic layer comprising a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals.

2. The method of claim 1 wherein the electroplated metallic layer comprises Cu.

3. The method of claim 1 wherein the electroplated metallic layer comprises Ag.

4. The method of claim 2 further comprising:

substantially removing electroplated copper overlying the opening and overlying the field, and removing the seed layers and the barrier layer overlying the field, wherein the removing comprises one or more of a mechanical polishing technique, a chemical mechanical polishing technique, a wet etching technique, and a dry etching technique.

5. The method of claim 1 wherein the first deposition technique comprises a conformal deposition technique and the second deposition technique comprises a non-conformal deposition technique.

6. The method of claim 5 wherein:

the conformal deposition technique comprises a chemical vapor deposition (CVD) technique or an electroless technique; and

the non-conformal deposition technique comprises a physical vapor deposition (PVD) technique.

7. The method of claim 5 wherein the conformal deposition technique is a chemical vapor deposition (CVD) technique.

8. The method of claim 1 wherein the first deposition technique comprises a non-conformal deposition technique and the second deposition technique comprises a conformal deposition technique.

9. The method of claim 8 wherein:

the non-conformal deposition technique comprises a physical vapor deposition (PVD) technique; and

the conformal deposition technique comprises a chemical vapor deposition (CVD or an electroless technique.

10. The method of claim 8 wherein the conformal deposition technique is a chemical vapor deposition (CVD) technique.

11. The method of claim 1 wherein the first and second seed layers comprise a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals.

12. The method of claim 5 wherein the first seed layer and the second seed layer comprise a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals.

13. The method of claim 8 wherein the first seed layer and the second seed layer comprise a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals.

14. The method of claim 1 wherein the first and second seed layers comprise Cu.

15. The method of claim 5 wherein the first and second seed layers comprise Cu.

16. The method of claim 8 wherein the first and second seed layers comprise Cu.

17. The method of claim 5 wherein the first seed layer has a thickness in a range of about 50Å to about 500Å over the field and the second seed layer has a thickness in a range of about 100Å to about 2,000Å over the field.

18. The method of claim 5 wherein the first seed layer has a thickness in a range of about 100Å to about 300Å over the field and the second seed layer has a thickness in a range of about 300Å to about 1,000Å over the field.

19. The method of claim 8 wherein the first seed layer has a thickness in a range of about 100 Å to about 2,000Å over the field and the second seed layer has a thickness in a range of about 50Å to about 500Å over the field.

20. The method of claim 8 wherein the first seed layer has a thickness in a range of about 300Å to about 1,000Å over the field and the second seed layer has a thickness in a range of about 100Å to about 300Å over the field.

21. The method of claim 1 wherein the barrier layer is selected from a group consisting of Ta, TaN_X, Cr, CrN_X, Ti, TiN_X, W, WN_X, or alloys comprising one or more of these materials.

22. The method of claim 1 wherein the barrier layer is deposited by a chemical vapor deposition technique.

23. The method of claim 1 wherein the barrier layer is deposited by a physical vapor deposition technique.

24. The method of claim 1 wherein the barrier layer has a thickness in a range of about 30Å to about 500Å.

25. The method of claim 1 wherein the barrier layer has a thickness in a range of about 50Å to about 300Å.

26. A method for making copper interconnects comprising:

forming a patterned insulating layer on a substrate, the patterned insulating layer including at least one opening and a field surrounding the at least one opening;

depositing a barrier layer over the patterned insulating layer including overlying the field and inside surfaces of the at least one opening, the barrier layer comprising a refractory metal or an alloy comprising a refractory metal;

chemical vapor depositing a first copper seed layer over the barrier layer, the first copper seed layer substantially continuously covering inside surfaces of the at least one opening;

physical vapor depositing a second copper seed layer over the first copper seed layer; and

electroplating copper over the second seed layer.

27. A method for making copper interconnects comprising:

forming a patterned insulating layer over a substrate, the patterned insulating layer including at least one opening and a field surrounding the at least one opening;

depositing a barrier layer over the patterned insulating layer including overlying the field and inside surfaces of the at least one opening, the barrier layer comprising a refractory metal or an alloy comprising a refractory metal;

physical vapor depositing a first copper seed layer over the barrier layer;

chemical vapor depositing a second copper seed layer over the first copper seed layer; and

electroplating copper over the second seed layer.

28. The method of claim 5 further comprising depositing at least one additional seed layer over the second seed layer prior to electroplating.

29. The method of claim 5 further comprising depositing at least one additional seed layer under the first seed layer.

30. The method of claim 28 wherein depositing at least one additional seed layer comprises using a conformal deposition technique.

31. The method of claim 29 wherein depositing at least one additional seed layer comprises using a non-conformal deposition technique.

32. The method of claim 30 wherein the first deposition technique comprises a chemical vapor deposition technique, the second deposition technique comprises a physical vapor deposition technique, and depositing at least one additional seed layer comprises using a chemical vapor deposition technique.

33. The method of claim 31 wherein depositing at least one additional seed layer comprises using a physical vapor deposition technique.

34. The method of claim 8 further comprising depositing at least one additional seed layer over the second seed layer prior to electroplating.

35. The method of claim 34 wherein depositing at least one additional seed layer comprises using a non-conformal deposition technique.

36. The method of claim 35 wherein the first deposition technique comprises a physical vapor deposition technique, the second deposition technique comprises a chemical vapor deposition technique, and depositing at least one additional seed layer comprises using a physical vapor deposition technique.

37. A method for making metallic interconnects comprising:

forming a patterned insulating layer on a substrate, the patterned insulating layer including at least one opening and a field surrounding the at least one opening;

depositing a barrier layer over the field and inside surfaces of the at least one opening;

depositing two or more seed layers over the barrier layer using two or more different deposition techniques; and

electroplating a metallic layer over the two or more seed layers, the electroplated metallic layer comprising a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals.

38. Copper filled via or trench interconnects on a substrate comprising:

a patterned insulating layer formed on the substrate, the patterned insulating layer including at least one opening;

a barrier layer formed over the patterned insulating layer, including inside surfaces of the at least one opening;

a first seed layer deposited over the barrier layer, including inside surfaces of the at least one opening;

a second seed layer deposited over the first seed layer; and

an electroplated metallic layer deposited over the second deposited seed layer, said metallic layer comprising a material selected from a group consisting of Cu, Ag, or alloys comprising one or more of these metals.

Abstract of the Disclosure

One embodiment of the present invention is a method for making metallic interconnects including: (a) forming a patterned insulating layer on a substrate, the patterned insulating layer including at least one opening and a field surrounding the at least one opening; (b) depositing a barrier layer over the field and inside surfaces of the at least one opening; (c) depositing a first seed layer over the barrier layer using a first deposition technique; (d) depositing a second seed layer over the first seed layer using a second deposition technique, the first and second deposition techniques being different; and (e) electroplating a metallic layer over the second seed layer, the electroplated metallic layer including a material selected from a group consisting of Cu, Ag, or alloys including one or more of these metals.

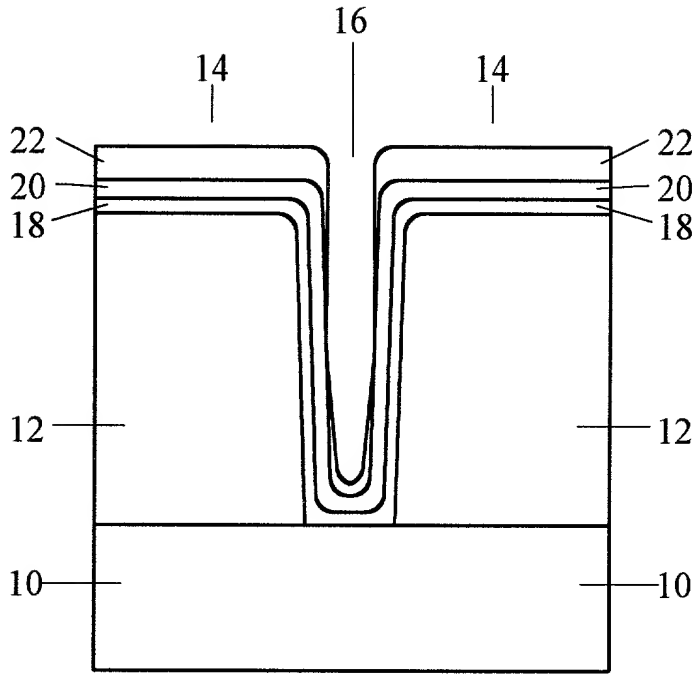

Figure 1

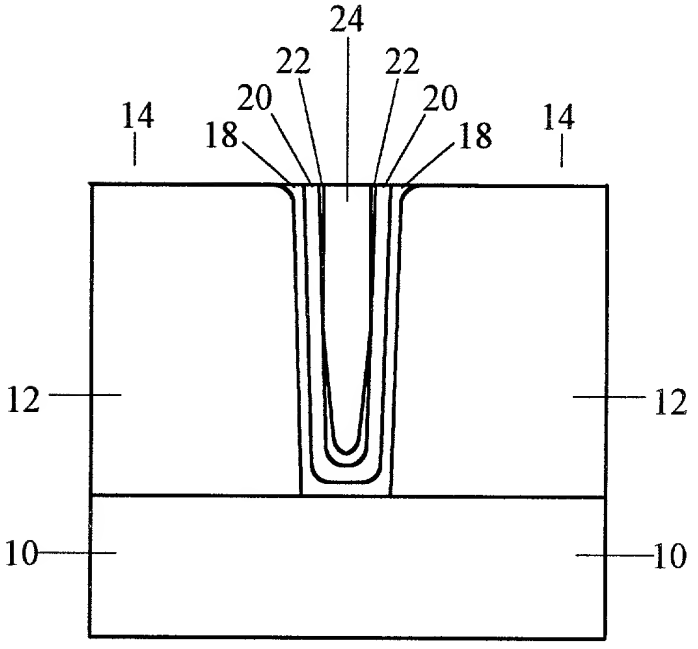

Figure 2

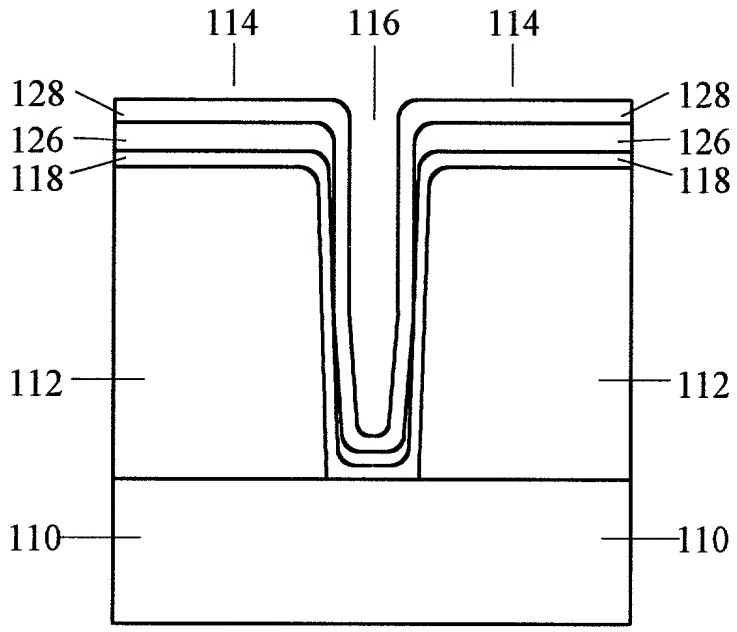

Figure 3

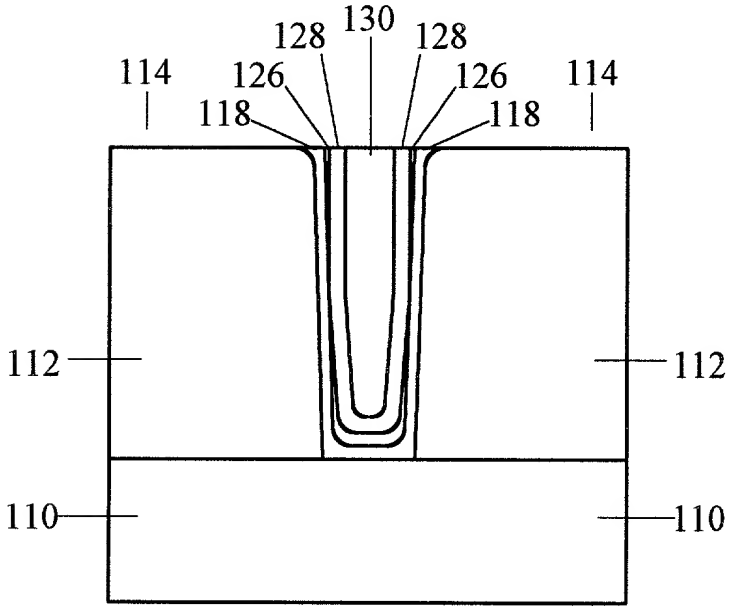

Figure 4

DECLARATION
(Utility Patent Application)

As a below named inventor, I hereby declare:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below), of the subject matter which is claimed and for which a patent is sought on the invention entitled:

Seed Layers for Interconnects and Methods for Fabricating Such Seed Layers

the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations section 1.56 (a).

I hereby claim foreign priority benefits under Section 119 of Title 35, United States Code for the above-identified US patent application based on the patent or inventor's certificate identified below and having a filing date before that of the US patent application for which priority is claimed:

Application No	Country	Filing Date	Priority Claimed under 35 USC 119
NONE			

I hereby claim the benefit under Section 120 of Title 35 of the United States Code of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by Section 112 of Title 35 of the United States Code, I acknowledge the duty to disclose material information, as defined in Section 1.56(a) of Title 37 of the Code of Federal Regulations, which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status Patented Pending Abandoned
NONE		

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Direct all telephone calls to: Uri Cohen at (650) 494-0268.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Citizenship: U.S.A. (country)

Signature: Uri Cohen Date: October 2, 1999